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Using the Digital I/O of your FPGA Module

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FPGA modules from HUNT ENGINEERING provide Digital I/O capability via one or more Digital I/O connectors on the module. The signals provided on the Digital I/O connectors are routed directly to the FPGA via series or parallel resistors for signal termination.

The FPGA modules support the use of many different I/O standards depending on the capabilities of the Xilinx FPGA that is fitted to each module.

The FPGA modules provide a variety of termination schemes varying from on-board parallel or series resistor networks or on-chip Digitally Controlled Impedance.

Single ended signalling is possible, as is differential signalling. When using a differential signalling standard such as LVDS for example, signals are paired on the connectors such that the associated positive and negative signal pairs can be used within the Xilinx FPGA.

This document details all of the issues involved in connecting to the Digital I/Os of your FPGA module including choice of termination scheme, I/O standard selection and differential signalling.

History

Rev 1.0	First written

Connecting to the Digital I/O

HUNT ENGINEERING provide example projects for each FPGA module. Example projects all use a common structure based around a Hardware Interface Layer. The Hardware Interface Layer is connected between the user logic inside the FPGA design and the real world signals outside the FPGA.

The Hardware Interface Layer is organised as a top level design file that is always named '`top.vhd`', and a set of VHDL modules that are responsible for interfacing to key functions such as DDR memory, Analogue-to-Digital devices, Digital-to-Analogue devices and HERON FIFO interfaces.

The example projects supplied with the modules instantiate a bi-directional LVTTL buffer for each of the digital I/Os. This is done in the top level design file `top.vhd`.

The Digital I/O connectors are labelled alphabetically starting at A. For each Digital I/O connector, the User-Ap interface to the Hardware Interface Layer will present three buses, each as wide as the number of bits of Digital I/O available on one connector.

The first bus is the input data received by the FPGA from the connector, and has a name in the form: `CONN_x_IN`, where 'x' is the connector label, for example '`A`' for connector A.

The second bus is the data output by the FPGA, and has a name in the form: `CONN_x_OUT`, where 'x' is the connector label.

The third bus is the output enable for the I/O buffer inside the FPGA, and has a name in the form: `CONN_x_EN`, where 'x' is the connector label.

For a board that has three digital I/O connectors, each with 30 digital I/O signals per connector, the signal entries in the User-Ap entity would appear as follows:

```
CONN_A_IN  : in  std_logic_vector(29 downto 0); -- Data input on Conn. A
CONN_A_OUT : out std_logic_vector(29 downto 0); -- Data output on Conn. A
CONN_A_EN : out std_logic_vector(29 downto 0); -- Output enables for Conn. A
CONN_B_IN : in  std_logic_vector(29 downto 0); -- Data input on Conn. B
CONN_B_OUT : out std_logic_vector(29 downto 0); -- Data output on Conn. B
CONN_B_EN : out std_logic_vector(29 downto 0); -- Output enables for Conn. B
CONN_C_IN : in  std_logic_vector(29 downto 0); -- Data input on Conn. C
CONN_C_OUT : out std_logic_vector(29 downto 0); -- Data output on Conn. C
CONN_C_EN : out std_logic_vector(29 downto 0); -- Output enables for Conn. C
```

The Output Enable bus is an active low bus. That is, for a Digital I/O to be an output from the FPGA, the corresponding output enable would be set to '0' in the user design. The following VHDL example shows how a logic '1' would be driven out on bit 4 of Digital I/O connector B:

```
CONN_B_OUT(4) <= '1'; -- Output a logic 1
CONN_B_EN(4)  <= '0'; -- Enable the output buffer
```

The following VHDL example shows how a digital input signal would be created for bit 8 of Digital I/O connector C:

```
Digital_Input <= CONN_C_IN(8); -- Input from bit 8
CONN_C_EN(8)  <= '1';          -- Disable the output buffer
```

Choosing The I/O Standard

The characteristics of the I/O are governed by the selections made in your FPGA design. Some signalling standards will need a Vref connected to the relevant pins of the FPGA, and some output buffers require a particular voltage to be provided on the Vcco pins of the FPGA bank. For a particular module, it might or might not be possible to provide the Vcco that you want.

By default, the buffers implement the default Select I/O standard for Xilinx FPGAs which is Low-Voltage TTL (LVTTL). The default buffers are also set to have an output current drive of 12mA and slow slew rate setting.

The I/O standard can be changed by adding component attributes to the buffer instantiations in the file `top.vhd`. The following VHDL shows the default buffer instantiation performed in `top.vhd`:

```
iDIOA0 : iobuf port map ( T  => CONN_A_EN(0),
                          I  => CONN_A_OUT(0),
                          O  => CONN_A_IN(0),
                          IO => dio_a(0) );
```

To change the I/O standard to something other than the default low-voltage TTL, the following VHDL should be added between the `architecture` and `begin` lines in the file `top.vhd`. The exact syntax will vary depending on the new I/O standard that is required. In this example, the I/O standard has been changed to Low-Voltage CMOS as follows:

```
attribute IOSTANDARD           : string;
attribute IOSTANDARD of iDIOA0 : label is "LVCMOS25";
```

To change the slew rate of the output buffers, the following VHDL would be used:

```
attribute FAST            : string;
attribute FAST of iDIOA0  : label is "TRUE";
```

To change the output drive, the following VHDL would be used:

```
attribute DRIVE           : string;
attribute DRIVE of iDIOA0 : label is "24";
```

Possible I/O Standards

Some output buffer types require a specific voltage to be connected to the Vcco pins of the FPGA bank containing the buffer.

Some modules have fixed Vcco voltages (because of other fixed signals connected to the same FPGA bank) and so will not support some of the signalling standards. Typically an input buffer doesn't require a Vcco, so these will be supported.

Some modules will offer a jumper, where the Vcco can be easily connected to one of the power supplies available on the module. Although more difficult it could be possible to connect another voltage level to the centre pin of the jumper to gain the possibility of other signalling standards.

The Xilinx user guide for each FPGA describes what Vcco setting must be used for each Select I/O standard. When choosing an I/O standard other than the LVTTL default it is important to refer to the available Vcco options for the module used.

It is also very important to note that most FPGA families cannot tolerate 5V signalling directly onto the pins of the FPGA.

Some HUNT ENGINEERING FPGA modules provide locations for series resistors to be fitted. These resistors enable 5V signals to be input to the FPGA. The series resistors in combination with input clamp diodes and the over-voltage protection devices limit the FPGA input to 3.3V, with the remaining input voltage being dropped across the series resistor.

The series resistors required for 5V connection must be requested when an FPGA module is ordered.

There is no way to provide 5V output signals from the module, but mostly 5V standards will accept the levels driven from LVTTL which is a 3.3V standard.

Signal Termination

When transmitting and receiving data it is very important to consider signal termination. Depending on the I/O standard that has been chosen the type and value of the termination will vary.

Properly terminating the Digital I/O signals can be done in one of two ways. Firstly, the FPGA modules provide locations for resistor packs so that groups of digital I/Os can receive series resistors or parallel termination resistors across a signal pair.

Secondly, with some FPGA modules it is possible to use the internal Digitally Controlled Impedance (DCI) feature of the Xilinx FPGA.

Using the Module Resistor Packs

Resistor packs can be fitted to some FPGA modules and can perform one of two functions. The first function is to provide a series resistance between the pin of the Digital I/O connector and the FPGA. The second function is to provide a parallel resistor between a pair of Digital I/O signals for terminating a differential connection.

It should be noted at this point that all FPGA modules are built as standard with a value of 0 Ohms for all series termination resistors, and with no parallel resistors fitted.

This means that if a particular termination scheme is required the fitting of resistors, and the values required must be specified at the time of ordering.

Using Digitally Controlled Impedance (DCI)

Most FPGA families allow the use of Digitally Controlled Impedance to control the impedance of certain I/O pins. For each FPGA I/O bank, the FPGA uses a pair of external resistors connected to the VRN and VRP pins of the FPGA to define the termination resistance value.

To use DCI the `IOSTANDARD` attribute must be applied to each I/O instance that requires the use of digitally controlled impedance. The following VHDL shows an example of how this would be done if a DCI LVDS buffers were required:

```
attribute IOSTANDARD           : string;
attribute IOSTANDARD of iDIOA0 : label is "LVDCI_33";
```

To correctly use DCI the right value of external resistance must be connected to the VRN and VRP pins of the FPGA. By default FPGA modules are fitted with 50 Ohm resistors to VRN and VRP. This is the value that is most widely used by the many different DCI I/O standards of Xilinx FPGAs. If a different DCI value is required this must be specified when the module is ordered.

Differential Signalling

The Xilinx FPGAs support differential signalling formats with I/O pins being grouped together to form the positive and negative signals of a differential signal pair.

The Digital I/O connectors on HUNT ENGINEERING FPGA modules are typically pinned out such that the differential signal pairs of the FPGA are on consecutive pins of the connector.

Differential Termination

Differential signalling standards need to be terminated with a resistor between the two halves of the differential pair.

Early Xilinx families provided this termination by terminating each half of the signal in a split termination (one to power and the other to ground). While this offers the correct equivalent termination as far as the AC signal is concerned, it also adds significantly to the static power supply current. For this reason HUNT ENGINEERING do not recommend using this method.

On boards that have FPGAs using this type of termination HUNT ENGINEERING have provided, external to the FPGA, true differential termination resistors. These must be soldered to the board for signals that will be used as differential inputs, and must not be soldered for differential outputs or single ended signals.

Later families of FPGAs implement a true differential termination that can be selected in your FPGA design. In this case HUNT ENGINEERING do not provide the differential termination resistors external to the FPGA.

When using the Camera Link example with FPGA families that have true differential termination the `DIFF_TERM` attribute must be used in the UCF file using the following syntax:

```
INST <I/O_BUFFER_INSTANTIATION_NAME> DIFF_TERM = “TRUE”;
```

Placing Differential Buffers

The example projects supplied with the modules instantiate one bi-directional LVTTL buffer for each digital I/O signal. When using differential signalling two digital I/Os must be connected to the same differential buffer for each differential connection.

The following VHDL example shows how the first two digital I/O signals on module Connector A would be converted into a differential input by modifying the top level design file `top.vhd`:

```
architecture RTL of TOP is

  component IBUFDS
    port( I  : in  std_logic;
          IB : in  std_logic;
          O  : out std_logic );
  end component;

begin

  ibuf0 : IBUFDS port map (I=>dio_a(1), IB=>dio_a(0), O=>Diff_Input);

end RTL;
```

The following VHDL shows how the first two digital I/O signals on module Connector A would be converted into a differential output:

```
architecture RTL of TOP is

  component OBUFDS
    port( I  : in  std_logic;
          O  : out std_logic;
          OB : out std_logic );
  end component;

begin

  obuf0 : OBUFDS port map (I=>Diff_Output, O=>dio_a(1),  OB=>dio_a(0));

end RTL;
```

For each differential signal pair there is a positive half and a negative half. For each FPGA the Xilinx documentation indicates whether a signal is the positive part of a pair with a P suffix in the I/O name or a negative part of a pair with the N suffix. For both signals in the differential pair the I/O number must match before the P or N suffix.