

'one of the many tools we have to help us build your system solution'



HERON-IO5-DO FPGA module with 2 channels of 12bit 210Mhz A/D and 2 channels of 16bit 160Mhz D/A with differential outputs

- HERON-IO5V-DO has Xilinx Virtex II FPGA with 1.5 or 3M gates
- FPGA configuration downloaded using the HERON Serial Bus.
- Choice of clocking options
- Two 210MSPS 12 bit A/Ds connected to the FPGA
- Two 160MSPS 16 bit D/As connected to the FPGA
- High analog signal bandwidth of 450Mhz in and 145Mhz out.
- 8 uncommitted digital I/Os
- Connects to all of the HERON FIFOs, UMI and module ID signals

The HERON-IO5 provides a user programmable FPGA along with fast Analog Inputs and outputs for a HERON system. The FPGA controls the sampling of the A/Ds and D/As. The incoming digitised data is then fed to the FPGA where it can be processed, buffered or simply written to a HERON FIFO for use in the rest of the system. The outgoing digitised data is then fed from the FPGA where it can be processed, buffered or simply read from a HERON FIFO.

Using the HERON serial bus allows the FPGA to be configured with a standard module configuration, or a custom one provided by the user or HUNT ENGINEERING. After configuration the module can accept user messages over the HERON serial bus, allowing registers etc to be programmed. If a more significant programming change is required a complete new FPGA configuration can be downloaded. The FLASH based configuration PROM can load the configuration data into the FPGA when it is used in an embedded system This PROM can be programmed using the standard JTAG cable available from Xilinx (such as Xilinx Parallel cable 4 or USB-JTAG cable).

The Digital I/O has a number of voltage formats such as LVTTL or LVCMOS defined by the configuration downloaded to the FPGA.

The HERON-IO5 can access HERON-FIFOs at a rate of 32 bits per FIFO clock in AND 32 bits per FIFO clock out concurrently. For example with a FIFO clock of 100Mhz this is 400Mbytes/sec in AND 400Mbytes/sec out.

The use of a Virtex II XC2V*fg676-6 part allows clock rates of up to 365Mhz, and also provides hard coded multipliers and extended I/O formats such as Low Voltage Differential Signalling (LVDS) NOTE VIRTEX II I/Os are not 5v tolerant!



Processor: Analog UP specifications Virtex II I Memory: In with common or independent clocking None external to FPGA Two connectors per channel: ultra-miniature 50 Ohm coaxial Hist Bus: Hirose UJFL-R-SMT Standard Input characteristics: AC coupled 50R, signal B/W from 200Hz to 450Mhz Zero input noise typically 3 levels maximum +8 levels (differential input mode) Input voltage +/-0.768mV Impedance form 50R to 1.7K Power requirements: V/C coupled choose I/P impedance between differential input mode) Typ: 300 mA D/C PFGA Power Consumption/Dissipation Max Bare FPGA package dissipation: 2.8W From 5V supply : FPGA PSU power can source 18.39W for Virtex II FPGA PSU power can source 18.39W for Virtex II D/C Clocking Speed: ADA 40MHz to 210Mhz ADA 40MHz to 210Mhz 2.2W Co fiste is required. Zero input noise typically 3 levels maximum +16 levels in differential input mode Analog OP specifications Channels Qurant distribution to 100Miz 2.8W Co fiste is required. Zero input noise typically 3 levels maximum +16 levels in differential input mode Manage OP specifications <t< th=""><th>Technical Specification</th><th></th><th>Ordering Information</th></t<>	Technical Specification		Ordering Information
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D/C - 50R, signal $B/W 0 - 145Mhz$		Optional Output types:	
		D/C - 50R, signal $B/W 0 - 145Mhz$	

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