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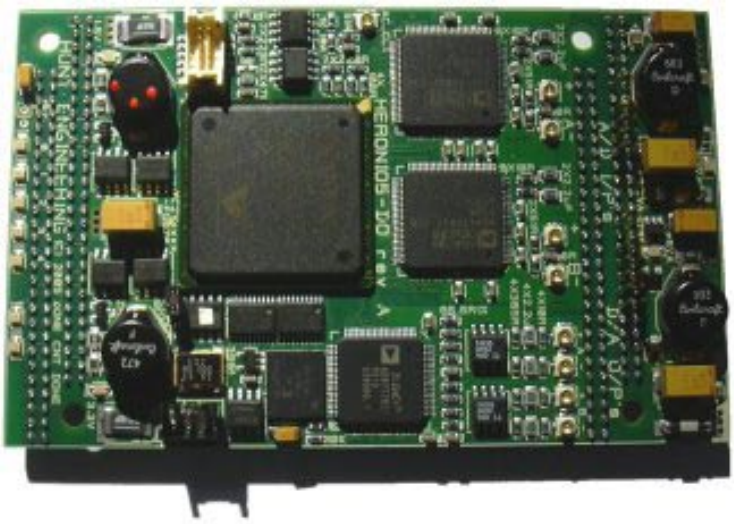
‘one of the many tools we have to help us build your system solution’



HERON-IO5-DO FPGA module with 2 channels of 12bit 210Mhz A/D and 2 channels of 16bit 160Mhz D/A with differential outputs

- **HERON-IO5V-DO has Xilinx Virtex II FPGA with 1.5 or 3M gates**
- **FPGA configuration downloaded using the HERON Serial Bus.**
- **Choice of clocking options**
- **Two 210MSPS 12 bit A/Ds connected to the FPGA**
- **Two 160MSPS 16 bit D/As connected to the FPGA**
- **High analog signal bandwidth of 450Mhz in and 145Mhz out.**
- **8 uncommitted digital I/Os**
- **Connects to all of the HERON FIFOs, UMI and module ID signals**

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The HERON-IO5 provides a user programmable FPGA along with fast Analog Inputs and outputs for a HERON system. The FPGA controls the sampling of the A/Ds and D/As. The incoming digitised data is then fed to the FPGA where it can be processed, buffered or simply written to a HERON FIFO for use in the rest of the system. The outgoing digitised data is then fed from the FPGA where it can be processed, buffered or simply read from a HERON FIFO.

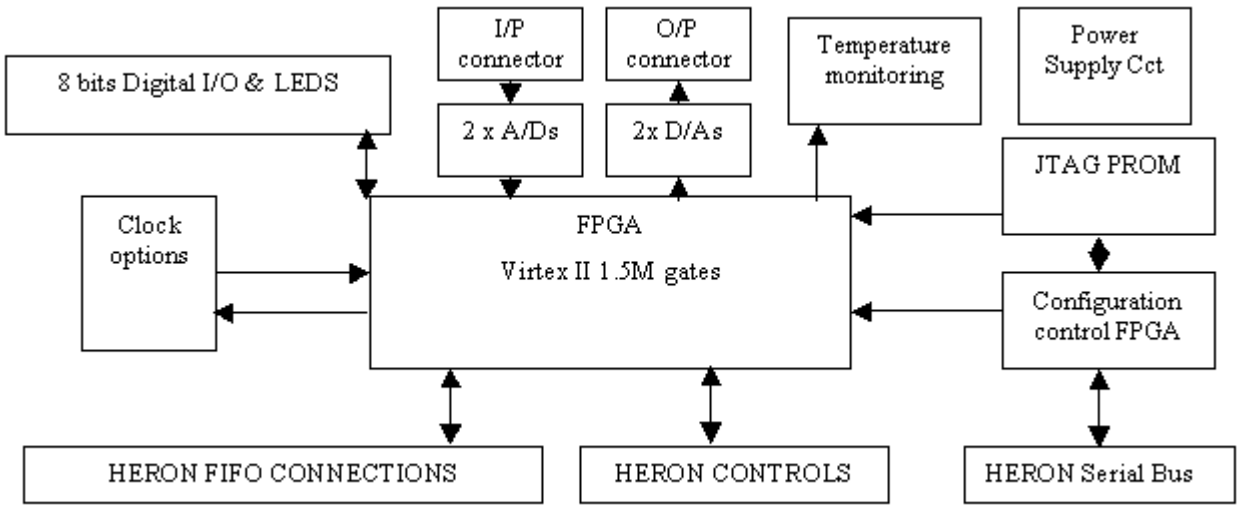
Using the HERON serial bus allows the FPGA to be configured with a standard module configuration, or a custom one provided by the user or HUNT ENGINEERING. After configuration the module can accept user messages over the HERON serial bus, allowing registers etc to be programmed. If a more significant programming change is required a complete new FPGA configuration can be downloaded. The FLASH based configuration PROM can load the configuration data into the FPGA when it is used in an embedded system This PROM can be programmed using the standard JTAG cable available from Xilinx (such as Xilinx Parallel cable 4 or USB-JTAG cable).

The Digital I/O has a number of voltage formats such as LVTTL or LVCMOS defined by the configuration downloaded to the FPGA.

The HERON-IO5 can access HERON-FIFOs at a rate of 32 bits per FIFO clock in AND 32 bits per FIFO clock out concurrently. For example with a FIFO clock of 100Mhz this is 400Mbytes/sec in AND 400Mbytes/sec out.

The use of a Virtex II XC2V*fg676-6 part allows clock rates of up to 365Mhz, and also provides hard coded multipliers and extended I/O formats such as Low Voltage Differential Signalling (LVDS)
NOTE VIRTEX II I/Os are not 5v tolerant!

Block diagram



Technical Specification		Ordering Information
Processor: Virtex II **Memory**: None external to FPGA **Host Bus:** HERON **Maximum Dimensions**: 4.0 inches x 2.5inches x 6.5mm high. **Power requirements:** 5V dependent on FPGA configuration 12V Max: 500 mA Typ: 300 mA **FPGA Power Consumption/Dissipation** Max Bare FPGA package dissipation: 2.8W From 5V supply : FPGA PSU power can source 18.39W for Virtex II Rest of logic uses 7.25W **Clocking Speed:** A/Ds 40Mhz to 210Mhz D/As 0hz to 160Mhz FPGA max: dependent on your FPGA design **I/O bandwidth:** e.g. HEPC9 400Mb/s in + 400Mb/s out	**Analog I/P specifications** **Channels** 2 in with common or independent clocking **Connectors** Two connectors per channel: ultra-miniature 50 Ohm coaxial Hirose U.FL-R-SMT **Standard Input characteristics:** A/C coupled 50R, signal B/W from 200Hz to 450Mhz Zero input noise typically 3 levels maximum 8 levels Offset typically +-3 levels maximum +-8 levels (differential input mode) Input voltage +/-0.768mV **Optional Input types:** **A/C** A/C coupled, with 50R on each input to ground as standard, but choose I/P impedance from 50R to 1.7K **D/C** D/C coupled choose I/P impedance between differential inputs from 50R to 1.7K, Signal B/W 0hz to 450Mhz but each input must not exceed the range 0v to +3.3V (of this module). This means a 2.8V DC offset is required. Zero input noise typically 3 levels maximum 10 levels Offset typically +-8 levels maximum +-16 levels in differential input mode **Analog O/P specifications** **Channels** 2 with common clocking. These converters are configurable over a serial bus to give functions including interpolation and modulation **Connectors** Two connectors per channel: ultra-miniature 50 Ohm coaxial Hirose U.FL-R-SMT **Standard Output characteristics:** Output voltage +/-2.1V differential A/C coupled 50R, signal B/W from 750Hz to 145Mhz **Optional Output types:** D/C – 50R, signal B/W 0 – 145Mhz	HERON-IO5V1500-DO Version with 1.5M gate Virtex II FPGA HERON-IO5V3000-DO Version with 3M gate Virtex-II FPGA

Distributor details: