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## *HERON-FPGA14 Virtex-4 LX60/SX35 FPGA module with 128Mbytes DDR SDRAM and 180 bits Digital I/O.*

- **Xilinx Virtex XC4VLX60 or Virtex XC4VSX35 FPGA**
- **128Mbytes of DDR SDRAM connected as 32Mx32 @200Mhz**
- **FPGA configuration downloaded using the HERON Serial Bus.**
- **Choice of clocking options**
- **180 bits of user programmable DIO**
- **Connects to all of the HERON FIFOs, UMI and module ID signals**
- **Flash PROM for storage of FPGA configuration data**

The HERON-FPGA14 provides a user programmable element for a HERON system combined with digital I/Os and SDRAM. The HERON-FPGA14 can be used as a hardware signal processing resource or as a flexible digital I/O module.

The module offers 128Mbytes of DDR SDRAM with 1.6Gbyte/sec total memory bandwidth. This off chip memory can be accessed from the FPGA logic. The provided Hardware Interface Layer (HIL) VHDL includes a DDR memory controller that can be connected to user FPGA logic.
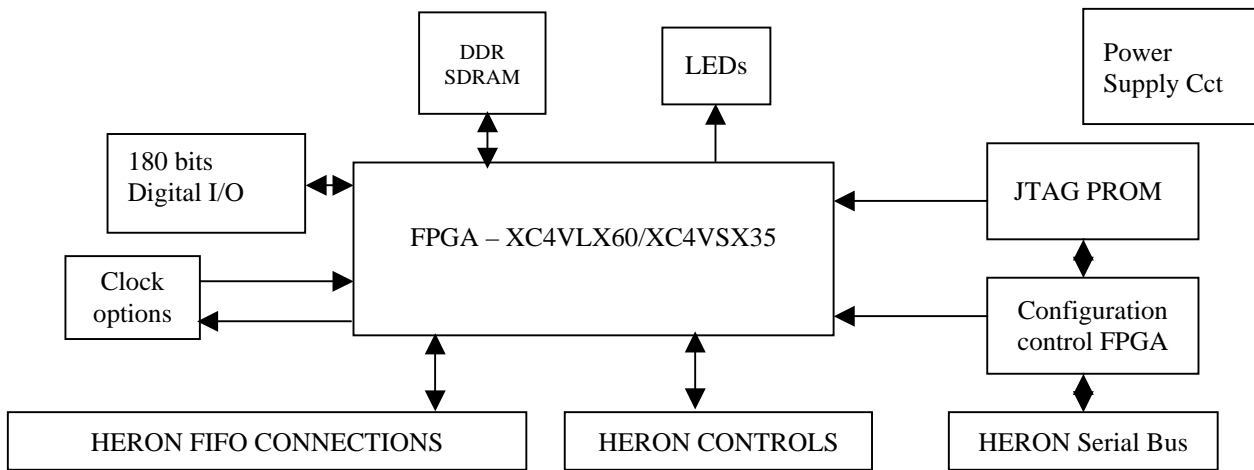
The module offers 180 bits of digital I/O. These I/Os can be configured by the FPGA design to use any Virtex-4 I/O format. 4 of the 6 connectors have a choice of Vcco, the remaining two connectors have their Vcco fixed at 3.3V.

HERON-FPGA modules must be fitted to a HERON module carrier that provides power and control signals to the module. Most module carriers also offer FIFO based connections between modules and possibly between the modules and a host PC. Normally the configuration program for the FPGA is sent from a host PC via the Heron Serial Bus, allowing fast development, test, debug cycles as well as in-field upgradeability. An alternative way of configuring the FPGA is the JTAG header that accepts standard Xilinx JTAG cables such as Xilinx Parallel cable 4 or USB-JTAG cable.

After configuration the Heron Serial Bus can be used for inter-module messages allowing FPGA registers to be read and written to control the operation of the module as defined in the FPGA design.

## Block Diagram

```
                   ┌──────────┐    ┌──────────┐                      ┌──────────────┐
                   │   DDR    │    │   LEDs   │                      │    Power     │
                   │  SDRAM   │    │          │                      │ Supply Cct   │
                   └────┬─────┘    └────┬─────┘                      └──────────────┘
   ┌──────────────┐     │               │                            ┌──────────────┐
   │  180 bits    │◄───►┌───────────────────────────────┐◄───────────│  JTAG PROM   │
   │  Digital I/O │     │                               │            └──────────────┘
   └──────────────┘     │  FPGA – XC4VLX60/XC4VSX35      │            ┌──────────────┐
   ┌──────────────┐────►│                               │◄───────────│Configuration │
   │    Clock     │     │                               │            │control FPGA  │
   │   options    │◄────└───────────────────────────────┘            └──────────────┘
   └──────────────┘          │              │
   ┌──────────────────────┐  ┌──────────────────┐   ┌──────────────────┐
   │ HERON FIFO CONNECTIONS│  │  HERON CONTROLS  │   │ HERON Serial Bus │
   └──────────────────────┘  └──────────────────┘   └──────────────────┘
```

| Technical Specification | Software | Ordering Information |
|---|---|---|
| **Processor**: <br> Virtex-4 XC4VLX60-11 <br> or <br> Virtex-4 XC4VSX35-11 <br> **Memory**: <br> DDR SDRAM 128Mbytes organised as 32M x 32 at 200Mhz <br> **Host Bus:** <br> HERON <br> **Maximum Dimensions**: <br> 4.0 inches x 2.5inches x 6.5mm high. <br> **Power requirements:** <br> 5V     Max: dependent on FPGA configuration <br>       Typ: dependent on FPGA Configuration <br> 12V    Max: 0A <br>       Typ: 0A <br> -12V   Max:0A <br>       Typ:0A <br> **FPGA Power Consumption/Dissipation** <br> Max Bare FPGA package dissipation: 2.9W <br><br> From 5V supply : <br> FPGA PSU power can source 12.5W <br> Rest of logic uses 0.6W <br><br> **Clocking Speed:** <br> FPGA Max: dependent on your FPGA design <br><br> **I/O bandwidth:** <br> e.g. HEPC9 400Mb/s in + 400Mb/s out | Xilinx ISE series tools are required to make a new FPGA configuration. HUNT ENGINEERING provides software to download the FPGA configuration file onto the hardware, plus configuration examples. HUNT ENGINEERING may offer to provide your configuration file for you, but this may be chargeable. <br><br> **Applications** <br> These fast FPGAs can be used for DSP processing tasks at very high clock rates. <br> Alternatively the HERON-FPGA12 can be used to provide custom digital I/O perhaps combined with signal generation, storage and pre-processing. <br><br> **Related Products** <br> HEPC9 – PCI Heron Module carrier <br> HERON-BASE2 – USB module carrier <br> HERON-IO series | HERON-FPGA14-LX60 <br> Or HERON-FPGA14-SX35 |

Distributor details:

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