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The HERON_IO2 Version 2 example4

Rev 1.1 P. Warnes 29-04-05

The HERON-IO2 module is a module that has an FPGA and 2 channels of fast A/D along with 2 channels of fast D/A.

Most users will use the FPGA to provide either a custom I/O capability or a processing resource that uses the FPGA for that processing. In that case the Example4 project can form a starting point for the development of that.

Example4 is provided for users who want to use the FPGA to handle and process data between the A/Ds and D/As, but will not interface with the HERON FIFOs. A user who is embedding a HERON-IO2 into a system is an example of this.

History

Example revision 1.0 10-05-02 document first written for HERON-IO2 Version 2

Example revision 1.2 29-04-05 Removed reference to specific ISE versions

What the bitstream does

The (Embedded Analogue I/O) example4 project for the HERON-IO2 is supplied on the HUNT ENGINEERING CD, along with the bitstream that can be loaded directly onto the HERON-IO2.

If you make changes to the project and re-build it you can change the functionality to be whatever you want, but if you use the supplied bit stream you need to know what it is doing:-

The standard clock soldered to “User Osc3” of the HERON-IO2 is 100Mhz. Example3 uses this clock to clock the A/D and D/A components.

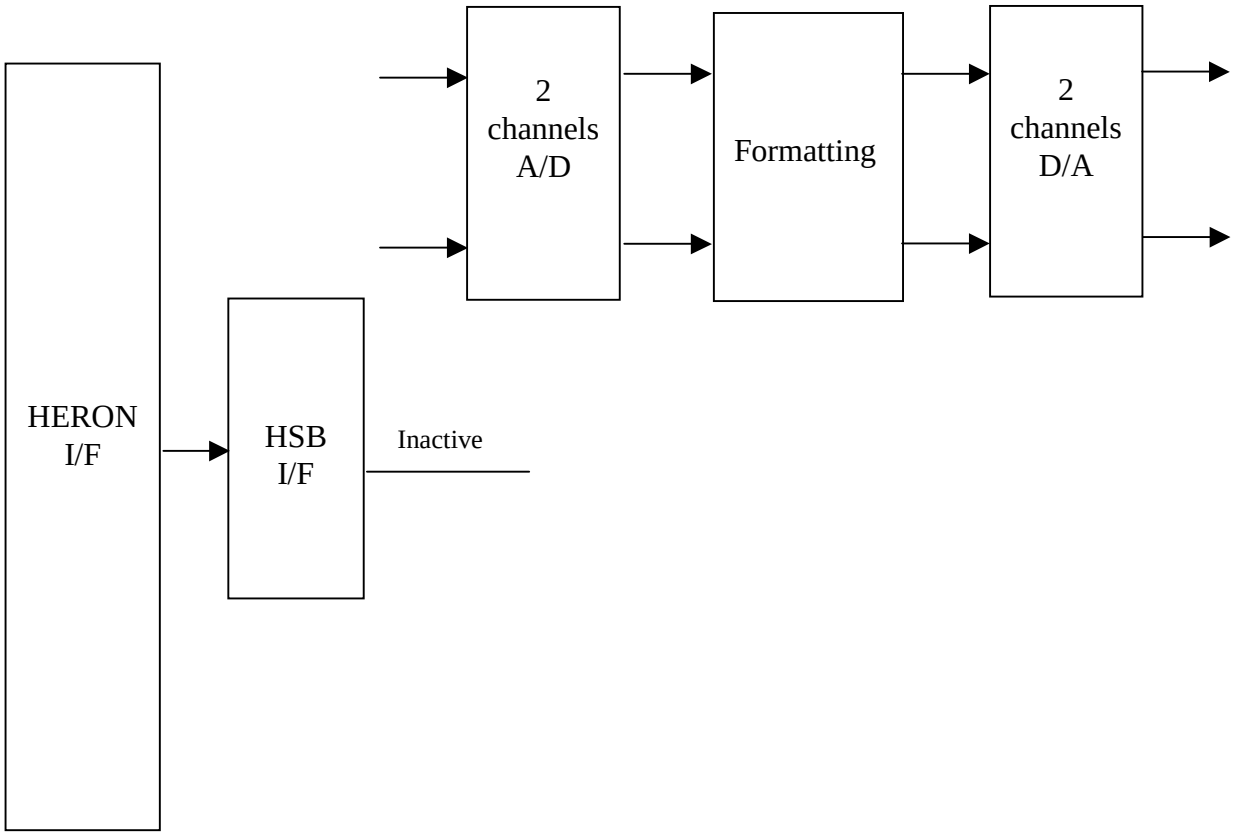
The bitstream uses both channels of A/D and both channels of D/A. The samples from A/D component A are replayed on D/A channel A, and the inputs from A/D B are simply replayed on D/A channel B.

Because the A/Ds are 12 bits, and use signed values, and the D/As are 14 bits using offset binary values, example4 inverts the top bit, and shifts the data up by 2 bits.

No use of the FIFOs are made, nor the HSB interface, but please note the HE_USER component is still placed and tied inactive to prevent unconnected signals being interpreted as a request to send an HSB message.

Example4 is a good confidence check for using with embedded modules. It can be configured into the FPGA using the HSB, or from the (optional) PROM. When the part is configured signals on the module analogue inputs should be seen re-constructed on the module analogue outputs.

FUNCTIONAL BLOCK DIAGRAM



Where are the bitstream and examples?

The bit streams for this example can be found on the HUNT ENGINEERING CD under \fpga\io2v2\embedded_IO(ex4). The name of the .rbt file reflects the FPGA part number i.e. 2s200fg456 is for the HERION-IO2S.

There are no DSP or host example as this is an example for stand alone use.

An easier way to navigate to the correct directory is to select the "Files" link next to the "Embedded Analog I/O" link under the IP sections of the CD browser.

The source files for the FPGA example can be found in the \src subdirectory. The sources in the \io2v2\common directory are also required. There is a project for ISE in the 'ISE' subdirectory.

FPGA example code

You should understand the HUNT ENGINEERING VHDL support for HERON modules before looking at this section. If you do not then please review example1 again (the getting started example for FPGA modules).

Example4 has some options in the user_ap4.vhdl file that allow you to select some options for the A/D clocking.

For example4 the SCLK_G_DOMAIN is set to True so that both A/Ds use the same clock source.

You need to consider the timing constraints that are defined in the .ucf file for your design. Actually if you use a time specification that is more strict than needed there is no problem, so the standard .ucf file have the clocks specified at 100Mhz. If the project builds (as example4 does) with this specification it is still guaranteed to work at lower clock speeds. If you add new clock nets into your design then you need to add new timing constraints into your design.