



HUNT ENGINEERING
Chestnut Court, Burton Row,
Brent Knoll, Somerset, TA9 4BP, UK
Tel: (+44) (0)1278 760188,
Fax: (+44) (0)1278 760199,
Email: sales@hunteng.co.uk
www.hunteng.co.uk
www.hunt-dsp.com



Using the HEGD11 with HERON FPGA modules

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The HERON-FPGA and HERON-IO families are ranges of HERON modules that have FPGAs. The FPGAs provided on these modules enable high performance digital signal processing to be performed in a HERON system.

The GDIO family is a range of modules that provide simple I/O interfaces including Analogue to Digital conversion and Digital to Analogue.

By using FPGA and GDIO modules together, A-to-D and D-to-A conversion can be combined with the FPGA processing of data.

This document discusses how to use FPGA based HERON modules to receive data from A-to-D GDIO modules and to send data to D-to-A GDIO modules.

A VHDL example template is given. The VHDL in the template is provided as a starting point for communication with the HEGD11 in your own FPGA design. The VHDL contained in the example templates will need to be cut and pasted to your project source as required.

History

Rev 1.0	First written
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Receiving Data from A-to-D GDIO Modules

The GDIO A-to-D modules output a continuous stream of sample data from one or more channels over a single HERON FIFO connection.

This document assumes that you have already correctly configured your system such that the A-to-D data is arriving on HERON Input FIFO 0 of your FPGA module. If you are using a different FIFO number then you will need to change the VHDL accordingly.

With A-to-D data being presented on HERON Input FIFO 0 the FPGA must read 32-bit words of FIFO data and separate that data into distinct A-to-D streams. For each A-to-D channel of the GDIO module one unique data stream must be created within the FPGA.

In the example template there is VHDL that unpacks and strips each channel of data from HERON Input FIFO 0. Data busses are created in either signed or unsigned formats, and unique clock enable signals are created for each channel of A-to-D data.

Using the HEGD11

The HEGD11 samples data on up to twelve channels. These channels are numbered from 0 to 11. Each channel is 12-bits in size, and the data is unsigned.

The example VHDL receives data from the HEGD11 on HERON Input FIFO 0 and automatically creates twelve unique data-valid/clock enable signals, one for each channel.

Two separate output buses are created. One for unsigned data from the HEGD11, and one that changes the top-bit to create signed sample data. In your own design either data bus may be used according to your own FPGA data format requirements.

The following table shows the output signals created by the example VHDL.

<u>VHDL Signal</u>	<u>Signal Function</u>
GD11_CH0_EN	Data Valid For Channel 0
GD11_CH1_EN	Data Valid For Channel 1
GD11_CH2_EN	Data Valid For Channel 2
GD11_CH3_EN	Data Valid For Channel 3
GD11_CH4_EN	Data Valid For Channel 4
GD11_CH5_EN	Data Valid For Channel 5
GD11_CH6_EN	Data Valid For Channel 6
GD11_CH7_EN	Data Valid For Channel 7
GD11_CH8_EN	Data Valid For Channel 8
GD11_CH9_EN	Data Valid For Channel 9
GD11_CH10_EN	Data Valid For Channel 10
GD11_CH11_EN	Data Valid For Channel 11
GD11_UNSG_DATA(11 downto 0)	12-bit Unsigned A-to-D Data
GD11_SGN_DATA(11 downto 0)	12-bit Signed A-to-D Data

