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Using the HEGD14 with HERON FPGA modules

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The HERON-FPGA and HERON-IO families are ranges of HERON modules that have FPGAs. The FPGAs provided on these modules enable high performance digital signal processing to be performed in a HERON system.

The GDIO family is a range of modules that provide simple I/O interfaces including Analogue to Digital conversion and Digital to Analogue.

By using FPGA and GDIO modules together, A-to-D and D-to-A conversion can be combined with the FPGA processing of data.

This document discusses how to use the HEGD14 D/A module with FPGA based HERON modules .

A VHDL example template is given. The VHDL in the template is provided as a starting point for communication with the HEGD14 in your own FPGA design. The VHDL contained in the example template will need to be cut and pasted to your project source as required.

History

Rev 1.0 First written

Sending Data to D-to-A GDIO Modules

The GDIO D-to-A modules expect a stream of sample data for one or more channels over a single HERON FIFO connection.

This document assumes that you have already correctly configured your system such that the data output on HERON Output FIFO 0 of your FPGA module is being received by the GDIO D-to-A module. If you are using a different FIFO number in your system you will need to change the VHDL accordingly.

The VHDL packs each channel into a single stream of data for HERON Output FIFO 0.

Using the HEGD14

The HEGD14 outputs data on up to eight channels. These channels are numbered from 0 to 7. Each channel is 14-bits in size, and the data is unsigned and negative. That is, a digital value of 0000h will give a +1 Volt output and a digital value of 3fffh will give a –1 Volt output.

The example VHDL expects a positive unsigned data value to be presented, and then negates that value to satisfy the requirements of the HEGD14.

Along with a 14-bit data bus, the example VHDL also expects a qualifying data valid/clock enable signal, and a last channel signal. It is up to the user logic to generate the data valid signal and last channel signal according to how sample data is to be output, and according to how many channels are to be output.

The example VHDL then generates a single FIFO output data stream on HERON Output FIFO.

The following table shows the input signals used by the example VHDL. These signals must be driven by logic created by the user.

VHDL Signal	Signal Function
GD14_CH_EN	Data Valid for all Channels
GD14_LAST_CH	Last Channel – Set high for last
GD14_UNS_DATA(13 downto 0)	14-bit Unsigned A-to-D Data