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RS232 ON FPGA MODULES

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The HUNT ENGINEERING FPGA modules include the appropriate drivers and receivers for implementing RS232. The logic required to generate and receive the RS232 signals could be written by the user, the Xilinx Core Generator offers another solution, or the RS232 interface in the digio examples can be used.

The HUNT ENGINEERING Digital I/O examples interface the RS232 to the Hunt Serial Bus (HSB) allowing the RS232 operating parameters to be downloaded over the HSB as well as sending and receiving data. This does not mean that if you want to use this RS232 interface that the HSB has to be used, the VHDL can be adapted to fix the operating parameters and the transmit and receive data routed elsewhere within the FPGA, for example to the HERON interface.

History

Example Rev 1.0	11-10-01	First written as document only
Example Rev 2.0	08-04-03	Rewritten using VHDL from digital I/O examples

What RS232 Is

RS232 is the connection commonly found as the Serial port of a PC. Many other types of equipment also use RS232, for example it is common that Digital Video Cameras use RS232 to allow user configuration of internal settings.

The RS232 standard defines the signal levels as well as the protocol used.

HERON modules with FPGAs have voltage level converters such as the MAX3160 that provide the correct voltage and current levels for the connection. It remains then to add the UART that provides the correct protocols – this can be made in the FPGA.

RS-232 Signals

The voltage converter chips IP provide a signal bi-directional RS-232 connection using the R1IN_A and T1OUT_A signals available on the Serial IO connector of the FPGA module.

Serial IO Connector	RS232 Signal
R1IN_A	RS-232 Input to the FPGA
T1OUT_A	RS-232 Output from the FPGA

Our example RS-232 UART uses these signals as TX and RX, and does not use the handshake signals RTS and CTS.

The RS-232 Interface uses a 16-byte transmit buffer and a 16-byte receive buffer. These buffers allow RS-232 transmission to be decoupled from the logic generating the messages.

The Baud rate of the RS-232 connection can be set using logic inputs to the UART.

VHDL Files

The files provided are VHDL source files that you can add to your own project.

The `RS232_uart.vhd` is the main file that implements the RS232 UART component.

That references the files `rs232rx.vhd` and `rs232tx.vhd`, each of which references the `ram16x8.vhd` file.

So you need to include all four files in your project.

Inputs and Outputs

The following signals are the interfaces to the RS232 UART component.

Signal	Type	Description
RESET	in std_logic	System reset to initialise the logic
CLOCK	in std_logic	Clock for logic. Must be supplied with a free running clock at 50MHz.
DIN	in std_logic_vector(7 downto 0)	Data to the TX FIFO
BAUD_SEL	in std_logic_vector(3 downto 0)	Baud rate of the RS-232 interface as follows: 0000 4800 0001 9600 0010 19200 0011 38400 0100 115200
STOP_BITS	in std_logic_vector(1 downto 0)	Number of stop bits to be used. (1 or 2)
RX	in std_logic	Serial data from voltage converter
READ	in std_logic	Control strobe to read from RX FIFO
WRITE	in std_logic	Control strobe to write to the TX FIFO
DOUT	out std_logic_vector(7 downto 0)	Data from the RX FIFO
TX	out std_logic	Serial data to the voltage converter
RX_EMPTY	out std_logic	There are no bytes to be read from the RX FIFO
TX_FULL	out std_logic	There are no spaces to write to the TX FIFO
RX_COUNT	out std_logic_vector(7 downto 0);	The number of data bytes that can be read from the RX FIFO
TX_COUNT	out std_logic_vector(7 downto 0)	The number of spaces in the TX FIFO

Using the RS232 UART in Your Design

You can instantiate and connect this component in your own design as long as you include the files in your project.

If you require more details you should look at the digital I/O examples for HERON-FPGA3 or 4 to see how the RS232 UART is used there.